Compact High-Efficiency Broadband Rectifier With Multi-Stage-Transmission-Line Matching

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***Abstract*—This brief proposes a compact high-efficiency broadband microwave rectifier for energy harvesting. The proposed rectifier is designed to operate over a broad bandwidth spanning from 2 to 3 GHz and an input power dynamic range from 0 dBm to 10 dBm. In the proposed structure, a compact broadband low-loss matching network and a dc-pass filter with a broad stopband were designed, leading to a high conversion efficiency in a wide frequency range with compactness. For the matching network, low loss and compact size were achieved by strategically choosing and designing three transmission line segments. Moreover, the proposed dc-pass filter is compact and can effectively block broadband RF signal and its in-band high order harmonics. Theoretical analysis and simulations of the proposed structure were carried out. A prototype was fabricated, which demonstrates a broadband bandwidth of 41.5% (2.0–3.05 GHz) where the RF-dc power conversion efficiency is higher than 70% at an input power of 10 dBm. The measured efficiency remains over 45% within 1.9–3.05 GHz when the input power decreases to 0 dBm. The maximum measured efficiency is 75.8% at an input power of 14 dBm.**

***Index Terms*—Broadband rectifier, compact low-pass filter, energy harvesting, multi-stage-transmission-line matching network, wireless power transfer.**

I. Introduction

THE ENERGY harvesting (EH) and wireless power transfer (WPT) technologies have been proved to be valuable for applications where wired power is unavailable or hard to access. In the past decade, EH technology has become increasingly popular with the rapidly growing wireless technologies, e.g., Wi-Fi, Bluetooth, 3G and 4G communication, etc. As abundant RF power is readily available in a typical urban environment, EH technology can extend the battery life of a wide range of electronic devices, including the wearable electronic devices, those for wireless sensor network, Internet of Things (IoT), and biomedical implanted devices [1]–[3].

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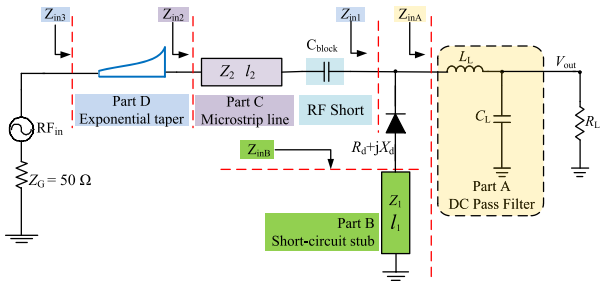


Fig. 1. The schematic diagram of the proposed broadband rectifier.

The available electromagnetic energy sources can be FM, DTV, 3G cellular or ISM 2.4 GHz devices, which span a wide frequency band. Besides, the power density of the available RF energy is time-varying. As a result, the operating frequency band of an EH rectifier should be sufficiently broad to collect as much energy as possible, and the rectifier should have a wide input power range. For the requirement on a broadband, both the antenna and the rectifier should be broadband. For a broadband antenna, multiple receive antennas working at different frequencies can be adopted. However, it is challenging to design a broadband rectifier with high efficiency. The reason is that a rectifier is nonlinear and its input impedance varies with both the input power and the operating frequency, which makes a broadband input impedance matching difficult. As a result, sophisticated matching networks are needed, which introduce additional insertion loss and lead to low RF-DC conversion efficiency (PCE).

Several research groups offered different design architectures to improve the performance of a rectifier over a broad bandwidth. Bolos *et al.* introduced one-octave bandwidth rectifier that is based on a nonuniform transmission line [4]. In this design, although the efficiency (η) remains above 60% from 470 to 860 MHz at an input power of 10 dBm, the long nonuniform transmission line introduces additional insertion loss, and meanwhile considerably increases the physical size of the device. In [5], a fractional bandwidth of 21.5% ($\eta > 70\%$) was realized by a second order branch-line coupler at the input. This structure exhibits a reasonable matching with a wide input power range, a wide frequency range, and a load dynamic range. However, the coupler introduces an insertion loss as high as about 0.9 dB, and takes up a relatively large circuit space, which compromises the efficiency and makes the device bulky. In [6], a two-level impedance matching network was proposed, this topology utilized a $\lambda/4$ transmission line terminated with two capacitors in parallel as an output DC-pass filter. Such an output DC-pass filter has a relatively narrow

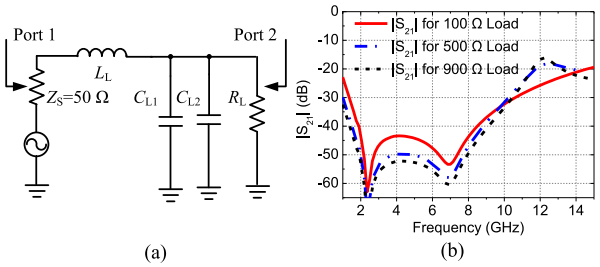


Fig. 2. The proposed DC-pass filter with a broad stopband. (a) The schematic. (b) Simulated $|S_{21}|$ versus frequency.

stopband. Consequently, it is highly possible that considerable RF power and the higher order harmonic components will leak to the load through the transmission line filter. In [7], a rectanna with a two-branch impedance matching circuit was proposed with enhanced performance and efficiency. In this design, the input RF power is divided into two branches and four diodes are used for rectification. Compared to a design with a single diode, this four-diode design is more lossy owing to the intrinsic loss of the diodes.

To have a broadband compact rectifier with high efficiency, a matching network with low insertion loss and compact size is important. Moreover, it is necessary to have a DC-pass filter that has a broad stopband and can prevent RF energy from leaking to the load when the load has parasitic inductance and/or capacitance, such as a DC-DC booster. In this brief, a novel compact high-efficiency broadband rectifier is proposed through the design of a compact, low-loss matching network in a broad bandwidth and a DC-pass filter with a broad stopband. The matching network is a three-stage transmission line that consists of three optimized transmission line segments in a designed sequence, with tapering transitions to avoid unnecessary radiation loss. The detailed design and theoretical analysis are presented in Section II. In Section III, the fabrication and measurement of the proposed rectifier are reported. A conclusion is drawn in Section IV.

II. Design and Simulation

Fig. 1 shows the schematic diagram of the proposed broadband rectifier. It consists of a DC-pass filter with broad stopband (Part A), a Schottky Diode, and a broadband matching network (Parts B, C and D). The center frequency f_c is set to be 2.5 GHz. The lower and upper bounds of the frequency of interest are denoted as f_1 and f_2, respectively.

A. Design of a DC-Pass Filter With a Broad Stopband, Part A

A DC-pass filter with a broad stopband at the output of the rectifier is needed to choke the RF signals within a wide frequency range. In [8], a $\lambda/4$ transmission line at f_c is terminated with a capacitor which is commonly used for "RF Choke". Such a conventional filter only chokes signals around f_c, but not those in a wide frequency range. Fig. 2 (a) shows the schematic of the proposed filter which blocks all in-band RF signal and passes the DC power to the load, R_L. The capacitors C_{L1} and C_{L2} are used in parallel to reduce the equivalent series resistance. when R_L is relatively large (>100 Ω), the cutoff frequency of this low-pass filter, f_{cut}, can be estimated by $1/2\pi\sqrt{LC_{sum}}$ where C_{sum} is the total capacitance of C_{L1} and C_{L2} [11].

In Fig. 2 (b), the simulated $|S_{21}|$ with different R_L are shown, $L_L = 10$ nH, $C_{L1} = 6.8$ pF, and $C_{L2} = 22$ pF. As shown, at different R_L's, $|S_{21}|$ is below −50 dB at f_c and is below −40 dB at the second and the third harmonics. The simulated $|S_{21}|$ shows that the leakage of RF power (including harmonics) to R_L is attenuated sufficiently by the proposed DC-pass filter.

B. Design of a Broadband Matching Network, Part B, C, & D

As shown in Fig. 1, the proposed broadband matching network for the diode consists of three transmission line segments, a short-circuit stub in Part B is proposed to reduce the imaginary part of the input impedance of the diode. A segment of a transmission line in Part C is proposed to further minimize the variation on the imaginary part of Z_{in1} over the whole frequency band of interest, and the input impedance after this modulation is denoted as Z_{in2}. The following Part D is an exponential taper transformer for matching Z_{in2} to 50 Ω.

1) Short Circuit Stub in Part B: The transmission line segment in Part B is a short-circuit stub that has the characteristic impedance of Z_1 and a length of ℓ_1. Its input impedance, Z_{inB}, is inductive. It is used to lower the imaginary part of the input impedance of the diode, Z_d, in the frequency band of interest. This technique was used in [9] and [10] for input impedance matching in a microwave rectifier. As shown in Fig. 1, Z_{in1} is expressed as

$$Z_{in1} = \frac{Z_{inA}(Z_d + Z_{inB})}{Z_{inA} + Z_d + Z_{inB}} \tag{1}$$

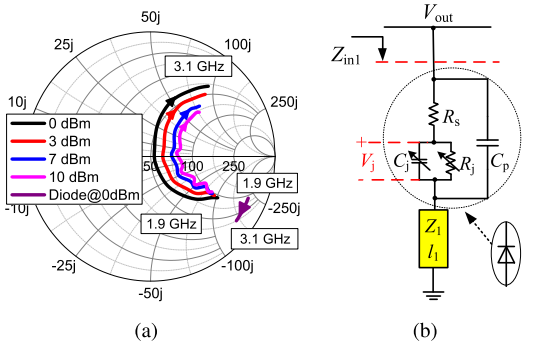
where Z_{inA} and Z_{inB} are the input impedance of Part A and B, respectively. With the DC-pass characteristics of the filter in Part A, $Z_{inA} = \infty$ at all frequencies of the input RF signal. With a short-circuit stub in Part B, $Z_{inB} = jZ_1 \tan\beta\ell_1$. Z_d is the impedance of the diode where $Z_d = R_d + jX_d$. Therefore, Z_{in1} can be rewritten as,

$$Z_{in1}(f) = R_d + jX_d + jZ_1 \tan\beta\ell_1 \tag{2}$$

In (2), $R_d + jX_d$ and therefore Z_{in1} are functions of both frequency and input power due to the non-linearity of the rectifying diode. Part B is designed to compensate the imaginary part of Z_d from f_1 to f_2, then, ideally, $Z_{in1}(f_1)$ to $Z_{in1}(f_2)$ on Smith Chart is a curve crossing the real axis and is symmetric along the axis. Therefore, at a given input power, Z_1 and ℓ_1 can be calculated by solving (3) below at f_1 and f_2.

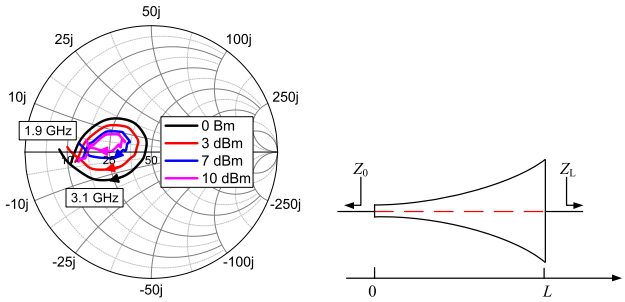
$$\mathrm{Im}(Z_{in1}(f_1)) = -\mathrm{Im}(Z_{in1}(f_2)) \tag{3}$$

In this broadband design, HSMS-2860 Schottky diode was chosen for its low build-in potential and low junction capacitance. The input impedance of HSMS-2860 diode with Part B was simulated using large signal S-parameter (LSSP) in Advance design system (ADS, Keysight) based on nonlinear diode model. Z_1 and ℓ_1 were calculated based on (3) and the specifications of the model of the diode. Fig. 3(a) shows the input impedance of HSMS-286 diode at 0 dBm, and Z_{in1} from 1.9 to 3.1 GHz at the input power of 0, 3, 7 and 10 dBm. The input impedance, Z_{in1}, at the lower ($f_1 = 1.9$ GHz) and upper bound ($f_2 = 3.1$ GHz) of the frequency band are tabulated in Table I. As can be seen, $\mathrm{Im}(Z_{in1})$ varies from −101.2 to 93.1 at 0 dBm and from −83.9 to 71.3 at 10 dBm. This indicates that the curve for the input impedance over the frequency band of interest is symmetric with respect to the real axis as



(a) (b)

Fig. 3. (a) Z_{in1} over 1.9-3.1 GHz at different input power levels. (b) Linear equivalent circuit for the diode with Part B.



(a) (b)

Fig. 4. (a) Z_{in2} over 1.9-3.1 GHz at different input power levels. (b) Schematic of the exponential tapered transformer.

TABLE I
INPUT IMPEDANCE Z_{in1}, Ω

Freq. GHz	0 dBm	3 dBm	7 dBm	10 dBm
1.9 (f_1)	92.9-101.2j	95.2-93.2j	97-86.5j	100-83.9j
3.1 (f_2)	38.5+93.1j	49.5+88.3j	64+75.9j	72.4+71.3j

TABLE II
INPUT IMPEDANCE Z_{in2}, Ω

Freq. GHz	0 dBm	3 dBm	7 dBm	10 dBm
1.9 (f_1)	11.1-2.9j	12.3-3.0j	13.3-3.0j	14.2-2.6j
3.1 (f_2)	7.8+0.7j	10.0+1.4j	13.6+2.6j	15.6+4.0j
2.5 (f_c)	40.0+13.6j	35.2+12.0j	30.5+9.9j	28.4+8.9j

designed. It is also noticed that within the frequency band of interest, Re(Z_{in1}) varies slightly with the increase of frequency, which is due to the junction capacitance C_j of diode (shown in Fig. 3(b)).

Besides, as shown in Fig. 3(a), Z_{in1} is power dependent because the parameters of a diode vary with the input power. Following is the explanation. Fig. 3(b) shows an equivalent circuit model for the diode with Part B. In the circuit, both the junction capacitance C_j and junction resistance R_j change their values with the input power. C_j is proportional to $1/\sqrt{(V_j + V_D)}$ where V_j is the junction voltage and V_D is the built-in voltage of diode. R_j is proportional to the diode turn-on angle which is also related to the input power and the load. C_p accounts for the packaging capacitance.

2) Impedance Transformer in Part C: The input impedance at Z_{in1} is further suppressed in the frequency band of interest using an impedance transformer in Part C. Before connecting the Part C, a DC-block capacitor (C_{block}) of 82 pF that has small reactance for the RF frequency of interest (an RF short) was inserted to block the DC voltage generated by the diode from reaching the generator. In Part C, the impedance transformer here is proposed to further reduce the imaginary part of Z_{in1}. It is a transmission line segment with a characteristic impedance of Z_2 (50 Ω) and a length of ℓ_2. The imaginary part of Z_{in1} will be suppressed to nearly zero by Part C. The input impedance is denoted as Z_{in2} after adding the Part C.

Based on transmission line theory, Z_{in2} can be obtained by going along the constant VWSR circle with certain electrical length starting from Z_{in1} on a smith chart. Mathematically, Z_{in1} and Z_{in2} are linked as follows,

$$Z_{in2}(f_i) = Z_2 \frac{Z_{in1}(f_i) + jZ_2 \tan\theta_2(f_i)}{Z_2 + jZ_{in1}(f_i)\tan\theta_2(f_i)} \quad i = 1, 2, c \tag{4}$$

$\theta_2(f_1)$ and $\theta_2(f_2)$ are the electrical length of Part C at f_1 and f_2, respectively. The ratio of the frequency is denoted as k, $k = f_2/f_1$ and $f_c = (f_1 + f_2)/2$. Therefore, $\theta_2(f_2)$ is linked to $\theta_2(f_1)$ and $\theta_2(f_c)$ in (5) below,

$$\theta_2(f_2) = k\theta_2(f_1) = \frac{2k}{1+k}\theta_2(f_c) \tag{5}$$

In the design, $\theta_2(f_1)$ and $\theta_2(f_2)$ were calculated by pushing $\mathrm{Im}(Z_{in2}(f_1)) \approx 0$ and $\mathrm{Im}(Z_{in1}(f_2)) \approx 0$, respectively. With an electrical length of 0.32λ at f_2, simulation was conducted for the diode with Part B and Part C. Z_{in2} was calculated. Fig. 4(a) shows the simulated Z_{in2} at different input power levels. As can be seen, after the impedance transforming in Part C, the four curves are bent towards the horizontal axis of Smith Chart, indicating a significant reduction in the imaginary part of the input impedance. Z_{in2} values at the upper and lower bounds were tabulated with an input power of 0, 3, 7 and 10 dBm in Table II. As shown in Table II, the imaginary part of the input impedance is reduced significantly whereas the real part is reduced to a range of 25±10 Ω.

3) Exponential Tapered Transmission Line in Part D: In order to match Z_{in2} to 50Ω in a broad bandwidth, Part D, an exponential tapered transmission line is proposed to match Z_{in2} to the source impedance. Fig. 4(b) shows an exponential tapered transmission line connecting to a source with an impedance of Z_0 at the input and connecting to Z_L at the output. The impedance along the z direction is expressed as

$$Z(z) = Z_0 e^{az}, \quad 0 < z < L, \tag{6}$$

where at $z = 0$, $z(0) = Z_0$, at $z = L$, $z(L) = Z_L = Z_0 e^{aL}$, and a is the exponential constant. In this design, $Z_0 = 50$ Ω and $Z_L = 25$ Ω which is an average value of the real part of Z_{in2}. The length of the tapered line was determined by minimizing the reflection coefficient at the input, $\Gamma(L) \leq 0.1$. $\Gamma(L)$ can be expressed by (7) below [12].

$$\Gamma(L) = \frac{1}{2}\int_0^L e^{-2j\beta z}\frac{d}{dz}(\ln(e^{az}))dz \tag{7}$$

Therefore, its magnitude is expressed as

$$|\Gamma(L)| = \frac{1}{2}\left|\ln\frac{Z_L}{Z_0}\right|\frac{\sin\beta L}{\beta L} \tag{8}$$

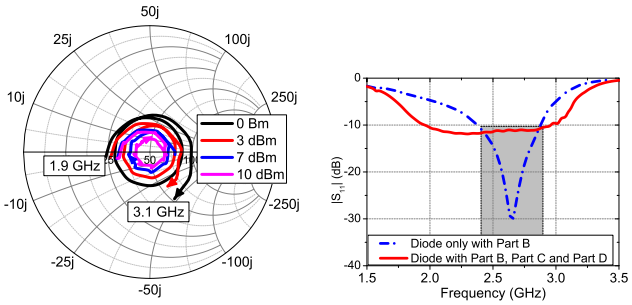


Fig. 5. (a) Z_{in3} over 1.9-3.1 GHz at different input power levels. (b) $|S_{11}|$ of a diode only with Part B and the one with Part B, C and D at 0 dBm.

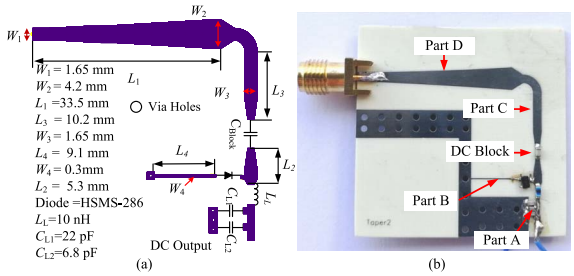


Fig. 6. The Proposed rectifier. (a) The layout. (b) A photograph.

with an assumption that the propagation constant β is not a function of z when a transverse electromagnetic line is assumed [12]. Based on (8), βL has to be greater than 0.73π to have $|\Gamma(L)|$ less than 0.1. Therefore, L was determined to be 0.73π at the lower bound of the frequency band at f_1.

Between Part D and Part C, tapering transmission line sections are used to avoid unnecessary radiation loss. The diode with the proposed Part B, C, and D was simulated and Z_{in3} was obtained. Fig. 5(a) shows the simulated Z_{in3} within the frequency band of interest at four input power levels. As can be seen, those curves are close to the 50 Ω on Smith Chart that implying matching is obtained in the frequency band which is from 1.9 to 3.1 GHz. For a comparison with the prior work in [9], Fig. 5(b) shows the input reflection coefficient $|S_{11}|$ for two devices, a diode only with Part B as that in [9] and the proposed one with Part B, C and D at 0 dBm input power. It can be seen that with Part B only, the good input matching at single frequency point can be achieved, whereas with the proposed Part B, C and D, the bandwidth for $|S_{11}|$ <10 dB is tripled. Furthermore, the matching network that consists of Part C and Part D was simulated to examine the insertion loss. Based on the simulation, the network shows an average insertion loss of 0.2 dB, which is much lower than the matching network for a broadband rectifier in [4] and [5].

III. Implementation and Measurements

The proposed broadband rectifier was fabricated for experimental validation. Rogers 4350B ($\epsilon_r = 3.66, \tan\delta = 0.002$, thickness = 0.762 mm) was used as the substrate. Fine optimizations are carried out using ADS program. The layout and the dimensions of the design are shown in Fig. 6, and a photograph of the fabricated circuit is also shown at the right side. In the experiment, the fabricated rectifier was measured in terms of efficiency versus input power and operating frequency. The

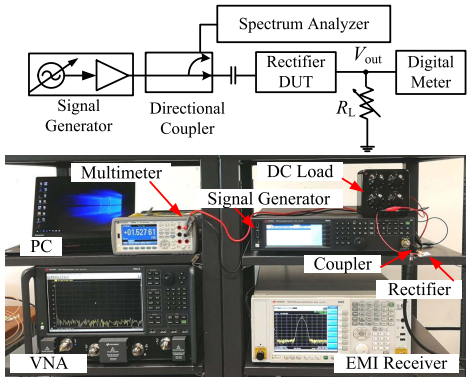


Fig. 7. The schematic and a photo of the experimental setup.

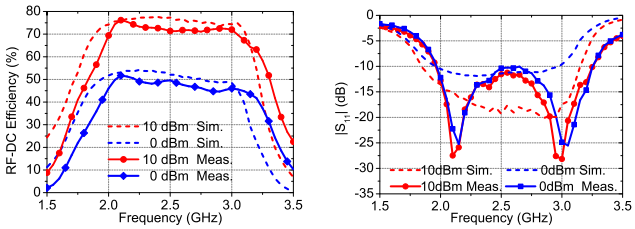


Fig. 8. Simulation and measurement results at the input power of 10 and 0 dBm. (a) PCE versus frequency. (b) $|S_{11}|$ versus frequency.

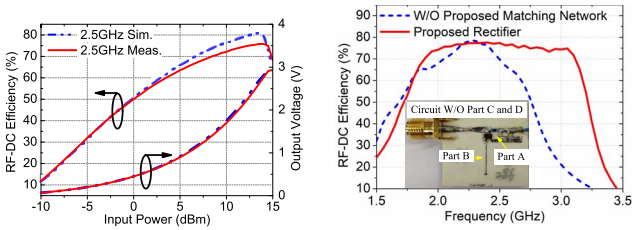


Fig. 9. (a) PCE and output voltage versus input power at the center frequency, 2.5 GHz. (b) Measured PCE for the proposed rectifier and the one without Part C and D.

measurements are compared with the simulation results in Fig. 8 and Fig. 9.

A. Implementation

For Part A, L_L, C_{L1} and C_{L2} were determined to be 10 nH, 22 pF, and 6.8 pF, respectively. According to (3), Z_1 and θ_1 of TL1 Part B were set to be 107 Ω and 43.5° at f_c, respectively. The characteristic impedance of TL2 in Part C is 50 Ω and θ_2 at f_c is determined to be 92.4° by using (4). Part C was bent to reduce the size of the proposed device. In Part D, the length of the exponential tapered transformer is 33.5 mm so that $\beta L > 0.73\pi$ is satisfied at f_1.

B. Measurement Results and Discussion

Fig. 7 shows the schematic (top) and a photo (bottom) of the experimental setup. An RF signal generator was used to feed the fabricated rectifier, and a direction coupler was connected between the signal generator and the rectifier. By varying the input power and frequency, the DC voltage V_{out} was measured across the load, $R_L = 400$ Ω. The measured efficiency was calculated by using (9) below. During the measurements, all

TABLE III
COMPARISON WITH SOME PRIOR RECTIFIERS

Ref	Efficiency over operating band			Max PCE (%)	Diode type & Circuit area (mm×mm)	Diode Num.
	PCE > 70%(GHz)	Frac. BW	Input power			
[4]	0	N.A	N.A	68% @10dBm	SMS7630 & 31×185	4
[5]	2.08-2.58	21.5%	17.2 dBm	80.8% @17dBm	HSMS286 & N.A	4
[6]	1.80-2.72	40%	19.5 dBm	80.3% @22dBm	HSMS282 & 60×25	1
[9]	1.8-2.62	37.1%	20 dBm	80.9% @20dBm	HSMS282 & 18×16	1
[14]	1.47-1.77	18.5%	10 dBm	80% @10dBm	HSMS286 & 71×20	2
This work	2.0-3.05	41.5%	10 dBm	75.8% @14dBm	HSMS286 & 36×35	1

the instruments are controlled by LXI (LAN eXtensions for Instrumentation) for automatic calibration and test.

$$\eta_{RF-DC} = \frac{P_{DC}}{P_{IN}} \times 100\% = \frac{V_o^2}{R_L} \times \frac{1}{P_{IN}} \times 100\% \qquad (9)$$

The simulated and measured efficiency versus operating frequency are plotted in Fig. 8(a). As can be seen, both the measured and the simulated efficiency are in good agreement. At the input power of 10 dBm, the measured efficiency is higher than 70% from 2.0 to 3.05 GHz, featuring a fractional bandwidth of 41.5%. When the input power is 0 dBm, the rectifier shows an efficiency that exceeds 45% from 2.0 to 3.05 GHz. The simulated results show the same bandwidth as that of the measured ones. As the frequency increases, the efficiency drops slightly, which is because parasitic impedance starts to play a role at the high frequencies and contributes to the loss. Furthermore, it is noticed that there is a frequency shift of 50 MHz between the simulation and measurement, which may be due to fabrication error and discrepancies between the diode model and the real device.

In Fig. 8(b), the simulated and measured $|S_{11}|$ at the input power of 10 and 0 dBm are shown. At 10 dBm, the measured $|S_{11}|$ is less than -10 dB from 1.95 to 3.25 GHz which corresponds to a fractional frequency bandwidth of 50%. The bandwidth for $|S_{11}| < 10$ dB at 0 dBm is the same as that at 10 dBm. It is observed that the matching at the middle frequency band is not as good as that in the simulation, which is mainly due to the discrepancy in impedance ratio of Part D between the simulation and the fabricated device. As can be seen in Fig. 6, the shape of the tapered line is altered by the soldered pin of a SMA connector, which changes the impedance ratio of the tapered line.

Fig. 9(a) depicts the efficiency and output voltage versus input power at 2.5 GHz. As shown, the measured and simulated efficiency are in good agreement. It can be seen that the maximum measured efficiency is 75.8% at 14 dBm. At a relatively high input power, the measured efficiency is lower than that in the simulation. The discrepancy is due to the fact that, in the simulation, only a finite number of harmonic components are included.

In order to show the effectiveness of the proposed matching network, Fig. 9(b) shows a comparison on efficiency between the proposed rectifier and the one without the matching network (Part C and D). As shown, with the proposed matching network, the bandwidth ($\eta > 70\%$) becomes twice as much as that without the matching network. The performance of the proposed work is compared to those of the main prior works featuring broadband in literature. Table III tabulates the performances. As shown, the proposed rectifier shows a fractional bandwidth ($\eta > 70\%$) of 41.5% which is the highest among all the designs under comparison. The number of diodes is kept to be one, and the physical size is 36×35 mm which is moderate under comparison.

IV. CONCLUSION

This brief presents a compact microwave broadband high-efficiency rectifier with an almost flat measured efficiency of over 70% from 2.0 to 3.05 GHz (41.5% fraction bandwidth) at an input power of 10 dBm. The proposed design maintains the same bandwidth for an efficiency higher than 45% at 0 dBm input power. The high performance is attributed to the novel low-loss broadband matching network which is a low-loss properly designed multi-stage-transmission-line network, and a compact DC-pass filter with a very broad stopband. The proposed rectifier has shown high-efficiency over a wide frequency range when compared to other reported broadband rectifiers. Furthermore, the rectifier has a compact size, and it is easy to fabricate. Besides EH, the proposed design can be applied to WPT, and simultaneous wireless information and power transfer. Future research includes optimizing this design at input powers below 0 dBm, and designing a broadband antenna working with the proposed rectifier.

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